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APPLICATION NO	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO	CONFIRMATION NO
10/023,350	12/20/2001	Dana A Chan	50432-528	5761

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McDERMOTT, WILL & EMERY
600 13th Street, N.W.
Washington, DC 20005-3096

EXAMINER
NGUYEN, DAO H

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 02/11/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/023,350	CHAN ET AL
	Examiner	Art Unit
	Dao H Nguyen	2818

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 December 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

[illegible] Priority under 35 U.S.C. §§ 120 and or 12[illegible]

Attachment(s)

1. ☒ Notice of References Cited, PTO-892
2. ☐ [illegible]

DETAILED ACTION

1. In response to the communications dated 12/20/2001, claims 1-19 are active in this application.

Specification

2. The specification has been checked to the extent necessary to determine the presence of possible minor errors. However, the applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

3. Claims 11 and 12 are objected to for the following reason:

Claims 11 and 12 recite the limitation "the isolating features" on line 1. There is insufficient antecedent basis for this limitation in the claims.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraph of 35 U.S.C. § 102 in view of the AIPA and H.R. 2215 that forms the basis for the rejections under this section made in the attached Office action:

> A person shall be entitled to a patent unless -
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language

5. Claims 1-4, 6-8, and 13-19 are rejected under 35 U. S. C. § 102 (b) as being anticipated by U.S. Patent No. 6,060,748 to Uchida et al.

Regarding to claim 1, Uchida et al. discloses a method of manufacturing a semiconductor device, as shown in figures 6, 8, 10 and 11, comprising the steps of:

providing a silicon layer over an insulating layer 12, the silicon layer including a first portion (the right portion) and a second portion (the left portion);

partially removing the first portion of the silicon layer, wherein a thickness of the second portion (the left portion) is greater than a thickness of the first portion (the right portion). See figures 10. and column 10. lines 10-67.

Regarding to claim 2, Uchida et al. discloses the method wherein the first and second portions of the silicon layer initially have the same thickness. See figure 10

Regarding to claim 3, Uchida et al. discloses the method wherein the step of partially removing the first portion of the silicon layer includes etching the first portion. See column 10, lines 17-35.

Regarding to claim 4, Uchida et al. discloses the method wherein the step of partially removing the first portion of the silicon layer includes depositing a resist over the silicon layer and exposing and developing the resist to expose the first portion of the silicon layer. See column 10, lines 17-35.

Regarding to claim 6, Uchida et al. discloses the method wherein the step of partially removing the first portion of the silicon layer includes oxidizing the first portion of the silicon layer and removing the oxidized silicon. See column 10, lines 31-39.

Regarding to claim 7, Uchida et al. discloses the method wherein the step of partially removing the first portion of the silicon layer includes depositing a mask layer and a resist over the silicon layer and exposing and developing the resist to expose a portion of the mask layer over the first portion of the silicon layer and removing the mask layer over the first portion of the silicon layer. See column 10, lines 25-35.

Regarding to claim 8, Uchida et al. discloses the method [illegible]

Regarding to claim 13, Uchida et al. discloses the method further comprising the step of forming a first transistor 32b in the first portion and the second transistor 31a in the second portion. See figures 6, 8.

Regarding to claim 14, Uchida et al. discloses the method wherein the first transistor includes first source/drain regions 19a/19b, and the second transistor includes second source/drain regions 13b, and a depth of the second source/drain regions 13b greater than a depth of the first source/drain regions 19a/19b. See figures 6, 8.

Regarding to claim 15, Uchida et al. discloses the method wherein the first transistor 32b includes source/drain regions 19a/19b formed with a first dopant (n-type), and the second transistor 31a includes source/drain region 13b formed with a second dopant (p-type), and the diffusivity of the second dopant into silicon is greater than the diffusivity of the first dopant into silicon. See figures 6, 8.

Regarding to claim 16, Uchida et al discloses a semiconductor, as shown in figures 6, 8, comprising:

an insulating layer 12;

a silicon layer over the insulating layer, the silicon layer including a first portion (right portion) and a second portion (left portion

portion. See figures

Regarding to claim 17, Uchida et al. discloses the device wherein a first transistor 32b is formed in the first portion and a second transistor 31a is formed in the second portion. See figures.

Regarding to claims 18, and 19, Uchida et al. discloses the device wherein the first transistor includes source/drain regions 19a/19b formed with a first dopant (n-type) and the second transistor includes source/drain regions 13b formed with a second dopant (p-type), and the diffusivity of the second dopant into silicon is greater than the diffusivity of the first dopant into silicon. See figures.

Claim Rejections - 35 U.S.C. § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth insection 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 5, 9-12 are rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. 6,060,748 to Uchida et al., in view of the following remarks.

Regarding to claim 5, Uchida et al. discloses a method comprising all the claimed

insulating layer 12 instead of by etching the first portion for a predetermined length of

time. However, it would have been an obvious matter of design choice to determine the thickness of the first portion by the insulating layer or by the time of etching or by any other methods, because those skilled in the art will recognize that various methods could be used to determine the thickness of the first portion without departing from the spirit of the invention of Uchida et al., In addition, the technique of determining thickness in etching semiconductor layer by etching time is well known in the art.

Regarding to claims 9 and 10, Uchida et al. discloses a method comprising all the claimed limitations. These are obvious matter of design choice.

Regarding to claims 11 and 12, Uchida et al. discloses a method comprising all the claimed limitations. These are obvious matter of design choice. See also column 10, lines 42-61.

Conclusion

8. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

A shortened statutory period for response to this action is set to expire 3 months

for response will cause the application to become abandoned (see M.P.E.P. 710.02(b)).

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dao H. Nguyen whose telephone number is (703) 305-1957. The examiner can normally be reached on Monday-Friday, 9 00 AM – 6:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (703) 308 - 4910. The fax numbers for Customer Service is (703) 872-9317, for the organization where this application proceeding is assigned is (703) 872-9318 for regular (Before Final) communications or (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

David Nelms
Supervisory Patent Examiner
Technology Center 2800

Dao H Nguyen
Art Unit 2818
January 31, 2003